SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORP
Form 6-K
September 07, 2006

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 6-K

REPORT OF FOREIGN PRIVATE ISSUER

Pursuant to Rule 13a-16 or 15d-16

under the Securities Exchange Act of 1934

For the month of September 2006

Commission File Number 1-31994

SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION

(Translation of Registrant s Name Into English)

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18 Zhangjiang Road

Pudong New Area, Shanghai 201203

People s Republic of China

(Address of Principal Executive Offices)

(Indicate by check mark whether the registrant files or will file annual reports under cover of Form 20-F or Form 40-F):

Form 20-F __X__ Form 40-F _____

(Indicate by check mark if the registrant is submitting the Form 6-K in paper as permitted by Regulation S-T Rule 101(b)(1)):

Yes _____ No __X__

(Indicate by check mark if the registrant is submitting the Form 6-K in paper as permitted by Regulation S-T Rule 101(b)(7)):

Yes _____ No __X__

(Indicate by check mark whether by furnishing the information contained in this Form, the registrant is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934):

Yes _____ No __X__

(If Yes is marked, indicate below the file number assigned to the registrant in connection with Rule 12g3-2(b): 82-____)

Semiconductor Manufacturing International Corporation (the Registrant) is furnishing under the cover of Form 6-K:

Exhibit 99.1:	Press release, dated September 6, 2006, entitled SMIC and Verisilicon Announced Release of a Standard Design Platform for SMIC s 0.13u Low Leakage Process.
Exhibit 99.2:	Press release, dated September 6, 2006, entitled Cadence and SMIC Deliver 90-Nanometer Low-Power Solution for Energy-Efficient SOC.

SIGNATURE

Pursuant to the requirements of the Securities Exchange Act of 1934, the Registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

Semiconductor Manufacturing International Corporation

By: /s/ Richard R. Chang
Name: Richard R. Chang
Title: President and Chief Executive Officer

Date: September 7, 2006

EXHIBIT INDEX

Exhibit	Description
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Exhibit 99.1

SMIC AND VERISILICON ANNOUNCED RELEASE OF A STANDARD

DESIGN PLATFORM FOR SMIC S 0.13u LOW LEAKAGE PROCESS

Library Release is Highly Optimized for Low Power, Low Leakage Applications

Shanghai, China, Sep. 6, 2006- VeriSilicon Holdings Co., Ltd. (VeriSilicon), a leading world class ASIC design foundry, semiconductor library and IP provider focusing on design and manufacturing services for customers worldwide, and Semiconductor Manufacturing International Corporation (SMIC) (NYSE: SMI; SEHK: 0981.HK), one of the leading foundry in the world jointly announced today the release of VeriSilicon s Standard Design Platform (SDP) for SMIC s 0.13um Low Leakage process. The SDP includes memory compilers for single port and dual port SRAM, Diffusion programmable ROM, Two-port Register File Compiler, standard cell library and I/O cell library.

This new SDP was optimized specifically for low leakage and low power, and has been proven in silicon through SMIC s 0.13um Low Leakage Silicon Shuttle Prototyping Service. In addition, the SDP supports industry-leading EDA tools, including Cadence, Synopsys, Magma and Mentor Graphics.

Several hundred customers worldwide have used VeriSilicon s Standard Design Platforms for their designs and many complex, multi-million gates SoCs have achieved first silicon success and started volume production. said Dr. Wayne Dai, chairman, President and CEO of VeriSilicon, We have developed low leakage and low power technologies for this newly released SDP, optimized specifically for SMIC 0.13um low leakage process; the technology can significantly reduce IC power consumption for optimal use in battery powered applications, such as handheld devices.

We thank VeriSilicon, one of our strategic partners continuous great support in the advancement of technology portfolio to serve our customers in China as well as in the world. said Richard Chang, President and CEO of SMIC, At the fast moving speed of the technology development, SMIC aims to work closely with VeriSilicon to deliver the excellence of the cooperation to the forefront of technology.

About SMIC

SMIC (NYSE: SMI; SEHK: 981) is one of the leading semiconductor foundries in the world and the largest and most advanced foundry in Mainland China, providing integrated circuit (IC) manufacturing service at 0.35mm to 90nm and finer line technologies. Headquartered in Shanghai, China, SMIC operates three 200mm fabs in Shanghai and one in Tianjin, and one 300mm fab in Beijing, the first of its kind in Mainland China. SMIC has customer service and marketing offices in the U.S., Italy, and Japan as well as a representative office in Hong Kong. For additional information, please visit http://www.smics.com.

About VeriSilicon

VeriSilicon Holdings Co., Ltd. is a leading world class ASIC design foundry providing libraries, semiconductor IPs, design and turnkey manufacturing services with multi-fab capability and on process technologies down to 90nm. VeriSilicon has achieved first silicon success and entered volume production of many complex, multi-million gates SoCs using the leading wafer foundries in APAC and China. VeriSilicon has operations in US, China, Taiwan, Japan, France, and Korea. Over 500 customers worldwide have licensed VeriSilicon IPs and Standard Design Platforms. In 2005, VeriSilicon was ranked number three in Deloitte Technology Fast 50 China, the top 50 fastest-growing technology companies in China and number six in Deloitte Fast 500 Asia Pacific, the top 500 fastest-growing technology companies in Asia Pacific. VeriSilicon was also named one of the Red Herring 100 Private Companies of Asia, and selected as one of the EE Times 60 Emerging Startups. For additional information, please visit http://www.verisilicon.com.

Safe Harbor Statements

(Under the U.S. Private Securities Litigation Reform Act of 1995)

Certain statements contained in this press release, such as statements regarding the ongoing cooperation between SMIC and VeriSilicon, may be viewed as forward-looking statements within the meaning of Section 27A of the U.S. Securities Act of 1933, as amended, and Section 21E of the U.S. Securities Exchange Act of 1934, as amended. Such forward-looking statements involve known and unknown risks, uncertainties and other factors (including without limitation the actual results of future cooperation between SMIC and VeriSilicon), which may cause actual events, and/or the actual performance, financial condition or results of operations of SMIC to be materially different from any future performance, financial condition or results of operations implied by such forward-looking statements. Further information regarding these risks, uncertainties and other factors is included in the Company s annual report on Form 20-F filed with the U.S. Securities and Exchange Commission (the SEC) on June 29, 2006 and such other documents that SMIC may file with the SEC or The Stock Exchange of Hong Kong Limited from time to time.

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Exhibit 99.2

CADENCE AND SMIC DELIVER 90-NANOMETER LOW-POWER SOLUTION FOR

ENERGY-EFFICIENT SOC

Cadence Encounter Timing System Adopted for SMIC s 90-nm Process

SAN JOSE, Calif. and SHANGHAI, China September 6, 2006 Cadence Design Systems, Inc. (NASDAQ:CDNS) and Semiconductor Manufacturing International Corporation (SMIC) (NYSE: SMI; SEHK: 0981.HK) today announced the companies have jointly developed the low-power digital reference flow to support SMIC s advanced 90-nanometer process technology. The reference flow, which includes support for the Cadence® Encounter® Timing System, is now available to address the increasing needs of designers developing ICs for the computing, consumer, networking and wireless markets.

The reference flow incorporates the Cadence Encounter digital IC design platform and Cadence Design for Manufacturing (DFM) technologies to address nanometer design challenges such as low power, complex hierarchical designs, timing and signal integrity (SI) signoff. The reference flow was developed using SMIC s 90-nanometer process technology and validated with sample designs. Cadence is one of the first electronic design automation company to launch a 90-nanometer RTL-to-GDSII reference flow with SMIC. New Cadence technologies, such as the Encounter Timing System, were incorporated into this flow for static timing analysis (STA) signoff.

Our collaboration with Cadence helps to drive our goal of continuing to enable the Chinese as well as global semiconductor market, said Paul Ouyang, vice president of Design Services at SMIC. As a leader in complex, low-power and digital design solutions, Cadence has provided its unique technology and expertise to create this reference flow . Mr. Ouyang continued, The 90-nanometer SMIC low power reference flow, fueled by Encounter Timing System and other advanced digital IC design technologies from Cadence, along with SMIC s process technologies, will ensure high levels of quality and productivity for our customers, and offers a faster, validated, reduced-risk path to silicon.

The SMIC-Cadence Reference Flow is a complete RTL-to-GDSII, low-power flow focused on efficient energy utilization for 90-nanometer system-on-chip (SoCs). It consists of power awareness throughout all necessary design steps, including logic synthesis, simulation, design for test, equivalence checking, silicon virtual prototyping, physical implementation and complete signoff analysis. Encounter low-power flow is one of the industry s first complete low-power solution for the modern energy efficient SoCs. The design, implementation and verification technologies are completely integrated to provide the designers with a big productivity boost. This reference flow deploys the Cadence Encounter wires-first continuous-convergence methodology and allows designers to quickly generate a feasible netlist and virtual prototype to identify and optimize power, timing, SI and routing early in the design cycle.

In addition, this flow provides a comprehensive platform for designers to drive RTL-to-GDSII with emphasis on fast, accurate and automatic timing, power and SI closure. It addresses hierarchical block partitioning, physical timing optimization, 3-D RC extraction, IR drop, leakage and dynamic power optimization, crosstalk glitch and delay analysis. This flow enables designers to architect and optimize advanced designs in a systematic, predictable way, providing the highest quality of silicon.

We are pleased to collaborate with SMIC and launch this reference flow based on its 90-nanometer process technology, said Mike McAweeney, vice president of business development of Industry Alliances at Cadence. Our engagement with SMIC puts in place another vital link in our customers design chain, ensuring a manufacturing aware design chain from idea to silicon. It also highlights the growing number of foundries and design houses in China that rely on the Cadence digital IC design flow.

The SMIC Cadence low-power digital reference flow offers a starting point to create energy-efficient, sub-130 nanometer SoCs. The flow incorporates several innovative Cadence technologies, including power aware design flow, Encounter Timing System, Encounter RTL Compiler global synthesis, SoC Encounter RTL-to-GDSII system, Cadence extraction technology, VoltageStorm® power analysis with PowerMeter functionality, and CeltIC® Nanometer Delay Calculator (NDC), using the highly accurate effective current source delay model (ECSM) to reduce time-to-volume for low-power consumer applications.

Availability

The SMIC and Cadence low-power digital reference flow kit is available to SMIC customers. SMIC customers may request the reference flow by contacting SMIC s Design Services at design_services@smics.com, or please contact your SMIC account manager.

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About Cadence

Cadence enables global electronic-design innovation and plays an essential role in the creation of today s integrated circuits and electronics. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2005 revenues of approximately $1.3 billion, and has approximately 5,100 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at www.cadence.com.

Safe Harbor Statements

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Company s annual report on Form 20-F filed with the U.S. Securities and Exchange Commission (the SEC) on June 29, 2006 and such other documents that SMIC may file with the SEC or The Stock Exchange of Hong Kong Limited from time to time.

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