XILINX INC
Form 10-K
June 01, 2009

UNITED STATES SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 10-K

(Mark One)
[X] Annual report pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934
For the fiscal year ended March 28, 2009.

[ ] Transition report pursuant to section 13 or 15(d) of the Securities Exchange Act of 1934
For the transition period from _____to_____.

Commission File Number 000-18548

Xilinx, Inc.

(Exact name of registrant as specified in its charter)

Delaware	**77-0188631**
(State or other jurisdiction of incorporation or organization)	(I.R.S. Employer Identification No.)
2100 Logic Drive, San Jose, CA	**95124**
(Address of principal executive offices)	(Zip Code)

(Registrant's telephone number, including area code) **(408) 559-7778**

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	**Name of each exchange on which registered**
Common stock, $0.01 par value	The NASDAQ Global Select Market

Securities registered pursuant to Section 12(g) of the Act: None

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. YES x NO o

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. YES o NO x

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. YES x NO o

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of the registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. x

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Website, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). YES x NO o

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer or a smaller reporting company. See the definitions of "large accelerated filer," "accelerated filer" and "smaller reporting company" in Rule 12b-2 of the Exchange Act.

Large accelerated filer x	Accelerated filer o	Non-accelerated filer o	Smaller reporting company o

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). YES o NO x

The aggregate market value of the voting stock held by non-affiliates of the registrant based upon the closing price of the registrant's common stock on September 27, 2008 as reported on the NASDAQ Global Select Market was approximately $4,798,431,000. Shares of common stock held by each executive officer and director and by each person who owns 5% or more of the outstanding common stock have been excluded in that such persons may be deemed affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

As of May 15, 2009, the registrant had 275,531,109 shares of Common Stock outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

Parts of the Proxy Statement for the Registrant's Annual Meeting of Stockholders to be held on August 12, 2009 are incorporated by reference into Part III of this Annual Report on Form 10-K.

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PART I

FORWARD-LOOKING STATEMENTS

This Annual Report on Form 10-K contains forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995. Forward-looking statements may be found throughout this Annual Report and particularly in Items 1. "Business" and 3. "Legal Proceedings" which contain discussions concerning our development efforts, strategy, new product introductions, backlog and litigation. Forward-looking statements involve numerous known and unknown risks and uncertainties that could cause actual results to differ materially and adversely from those expressed or implied. Such risks include, but are not limited to, those discussed throughout this document as well as in Item 1A. "Risk Factors." Often, forward-looking statements can be identified by the use of forward-looking words, such as "may," "will," "could," "should," "expect," "believe," "anticipate," "estimate," "continue," "plan," "intend," "project" and other similar terminology, or the negative of such terms. We disclaim any responsibility to update or revise any forward-looking statement provided in this Annual Report or in any of our other communications for any reason.

ITEM 1. BUSINESS

Xilinx, Inc. (Xilinx or the Company) designs, develops and markets complete programmable logic solutions. These solutions have several components:

- Advanced integrated circuits (ICs) in the form of programmable logic devices (PLDs);
- Software design tools to program the PLDs;
- Predefined system functions delivered as intellectual property (IP) cores;
- Design services;
- Customer training; and
- Field engineering and technical support.

Our PLDs include field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs) that our customers program to perform desired logic functions. Our solutions are designed to provide high integration and quick time-to-market for electronic equipment manufacturers in end markets such as wired and wireless communications, industrial, scientific and medical, aerospace and defense, audio, video and broadcast, consumer, automotive and data processing. We sell our products globally through independent domestic and foreign distributors and through direct sales to original equipment manufacturers (OEMs) by a network of independent sales representative firms and by a direct sales management organization.

Xilinx was founded and incorporated in California in February 1984. In April 1990, the Company reincorporated in Delaware. Our corporate facilities and executive offices are located at 2100 Logic Drive, San Jose, California 95124, and our website address is www.xilinx.com.

Industry Overview

There are three principal types of ICs used in most digital electronic systems: processors, which generally are utilized for control and computing tasks; memory devices, which are used for storing program instructions and data; and logic devices, which generally are used to manage the interchange and manipulation of digital signals

within a system. Xilinx develops PLDs, a type of logic device. Alternatives to PLDs include custom gate arrays, application specific integrated circuits (ASICs) and application specific standard products (ASSPs). These devices all compete with each other since they may be utilized in many of the same types of applications within electronic systems. However, variations in unit pricing, development cost, product performance, reliability, power consumption, density, functionality, ease of use and time-to-market determine the degree to which the devices compete for specific applications.

The primary advantage PLDs have over custom gate arrays, ASICs and ASSPs is that PLDs enable faster time-to-market because of their shorter design cycles. Users can program the PLD to implement their design, using software to create and revise their designs relatively quickly with lower development costs. PLDs typically have a larger die size resulting in higher costs per unit compared to custom gate arrays, ASICs and ASSPs, which are customized to perform a limited fixed function. Custom gate arrays, ASICs and ASSPs, however, generally offer less flexibility, require longer design cycles and higher up-front costs than PLDs.

PLDs are standard components. This means that the same device type can be sold to many different users for many different applications. As a result, the development cost of PLDs can be spread over a large number of users. Custom gate arrays, ASICs and ASSPs, on the other hand, are custom chips for an individual user for use in a specific application. ASSPs implement specific functions for a limited set of users. This involves a high up-front cost to users. Technology advances are enabling PLD companies to reduce costs considerably, making PLDs an increasingly attractive alternative to custom gate arrays, ASICs and ASSPs.

An overview of typical PLD end market applications for our products is shown in the following table:

End Markets	Sub-Segments	Applications
Communications	Wireless	• 3G/4G Base Stations • Wireless Backhaul
	Wireline	• Metro Area Networks • Optical Networks • Enterprise Switches • Mid-end and High-end Routers
Consumer, Automotive, Industrial and Other	Consumer	• Flat-Panel Televisions • Digital Video Recorders • Cable Set-Top Boxes
	Automotive	• GPS Navigation Systems • Rear-Seat Entertainment • Vision-Based Driver Assistance Systems
	Industrial, Scientific and Medical	• Factory Automation • Medical Imaging • Test and Measurement Equipment
	Audio, Video and Broadcast	• Cable Head-end Systems • Broadcast Equipment • Video Cameras
	Aerospace and Defense	

		• Satellite Surveillance • Radar and Sonar Systems • Secure Communications
Data Processing	Storage and Servers	
		• Security and Encryption • Computer Peripherals
	Office Automation	
		• Copiers • Printers

Products

Integral to the success of our business is the timely introduction of new products that meet customer requirements and compete effectively with respect to price, functionality, power and performance. Software design tools, IP cores, reference platforms, technical support and design services are also critical components that enable our customers to implement their design specifications into our PLDs. Altogether, our PLDs and related tools, IP, service and support form a comprehensive programmable logic solution. A brief overview of our PLD offerings follows and is not all-inclusive but does comprise the majority of our revenues. Some of our more mature product families have been excluded from the table although they continue to generate revenues. We operate and track our results in one operating segment for financial reporting purposes.

Product Families

FPGAs	Date Introduced	Densities	Process Technology	Voltage
Virtex®-6	February 2009	75K to 760K Logic Cells	40-nanometer (nm)	1.0v, 0.9v
Virtex-5	May 2006	20K to 330K Logic Cells	65nm	1.0v
Virtex-4	June 2004	12K to 200K Logic Cells	90nm	1.2v
Virtex-II Pro	March 2002	3K to 99K Logic Cells	130nm	1.5v
Virtex-II	January 2001	576 to 104K Logic Cells	150nm	1.5v
Virtex-E	September 1999	1.7K to 73K Logic Cells	180nm	1.8v
Spartan®-6	February 2009	4K to 150K Logic Cells	45nm	1.2v, 1.0v
Spartan-3A	December 2006	1.6K to 54K Logic Cells	90nm	1.2v
Spartan-3E	March 2005	2.2K to 33.2K Logic Cells	90nm	1.2v
Spartan-3	April 2003	1.7K to 75K Logic Cells	90nm	1.2v
Spartan-IIE	November 2001	1.7K to 16K Logic Cells	150nm	1.8v

CPLDs	Date Introduced	Densities	Process Technology	Voltage
CoolRunner™-II	January 2002	32 to 512 Macrocells	180nm	1.8v
CoolRunner	August 1999	32 to 512 Macrocells	350nm	3.3v

Virtex FPGAs

The Virtex-6 FPGA family consists of 13 devices and is the sixth generation in the Virtex series of FPGAs. Virtex-6 FPGAs are fabricated on a high-performance, 40-nm process technology. The Virtex-6 family is comprised of three domain-optimized platforms to deliver different feature mixes to address a variety of markets as follows:

- LXT platform: for applications that require high-performance logic, digital signal processing (DSP), and serial connectivity;
- SXT platform: for applications that require ultra high-performance DSP and serial connectivity;
- HXT platform: for communications applications that require the highest-speed serial connectivity.

The Virtex-5 FPGA family consists of 26 devices and five platforms: Virtex-5 LX FPGAs for logic-intensive designs, Virtex-5 LXT FPGAs for high-performance logic with serial connectivity, Virtex-5 SXT FPGAs for high-performance DSP with serial connectivity, Virtex-5 FXT FPGAs for embedded processing with serial connectivity and Virtex-5 TXT FPGAs for high-bandwidth serial connectivity.

Prior generation Virtex families include Virtex-4, Virtex-II Pro, Virtex-II, Virtex-E and the original Virtex family.

Spartan FPGAs

The sixth generation in the Spartan FPGA series, the Spartan-6 FPGA family, is fabricated on a low-power 45-nm process technology. The Spartan-6 family is the PLD industry□s first 45-nm high-volume FPGA family. The family consists of 11 devices and is delivered on two FPGA platforms to address diverse market and application requirements as follows:

- LX platform: for applications that require cost-effective logic, memory and DSP;
- LXT platform: for applications that require LX features plus high-speed serial transceivers.

Spartan-3 FPGAs were the PLD industry□s first 90-nm FPGAs and are comprised of three platforms including the original Spartan-3 family, the Spartan-3E family and the Spartan-3A family.

Prior generation Spartan families include Spartan-IIE, Spartan-II, Spartan XL and the original Spartan family.

EasyPath FPGAs

EasyPath□ FPGAs use the same production masks and fabrication process as standard FPGAs and are tested to a specific customer application to improve yield and lower costs. As a result, EasyPath FPGAs provide customers with significant cost reduction when compared to the standard FPGA devices without the conversion risk, conversion engineering effort or the additional time required to move to an ASIC. EasyPath FPGAs are available for the higher density devices of the Virtex-II Pro, Virtex-4 and Virtex-5 families. EasyPath FPGAs will also be available for the higher densities of the Virtex-6 family. Customers purchasing EasyPath FPGAs must meet certain minimum order requirements and pay a custom test generation charge.

CPLDs

CPLDs operate on the low end of the programmable logic density spectrum. CPLDs are single chip, nonvolatile solutions characterized by instant-on and universal interconnect.

The CoolRunner-II family is the latest generation Xilinx CPLD family with six devices in production. CoolRunner-II CPLDs combine the advantages of ultra low power consumption with the benefits of high performance and low cost. While CoolRunner-II is suitable for a wide variety of end markets and applications, the ultra low power consumption and small package profiles of these devices have led to their acceptance in the growing portable consumer electronics marketplace.

Prior generation CPLD families include the CoolRunner, XC9500 and XC9500XL, which offer low cost, high performance and in-system programmability for 5.0-volt and 3.3-volt systems, respectively.

Support Products

Targeted Design Platforms

We offer Targeted Design Platforms comprised of reference designs, target boards, application software, design tools, IP and silicon to reduce our customers development effort. Targeted Design Platforms are organized into three levels: the Base Platform; the Domain-Specific Platform; and the Market-Specific Platform to offer customers flexibility, accessibility, applicability and time-to-market.

The Base Platform is the delivery vehicle for all new silicon offerings used to develop and run customer-specific software applications and hardware designs. Released at launch, the Base Platform is comprised of: FPGA silicon; ISE® (Integrated Software Environment) Design Suite design environment; third-party synthesis, simulation, and signal integrity tools; reference designs; development boards and IP.

The Domain-Specific Platform targets one of the three primary Xilinx FPGA user profiles: the embedded processing developer; the DSP developer; or the logic/connectivity developer. It accomplishes this by augmenting the Base Platform with a targeted set of integrated technologies, including: higher-level design methodologies and tools; domain-specific IP including embedded, DSP and connectivity; domain-specific development hardware and reference designs; and operating systems and software.

The Market-Specific Platform enables software or hardware developers to quickly build and run their specific application or solution. Built for specific markets such as automotive, consumer, aerospace and defense, communications, audio, video and broadcast, industrial, or scientific and medical, the Market-Specific Platform integrates both the Base and Domain-Specific Platforms with higher targeted applications elements such as IP, reference designs and boards optimized for a particular market.

Design Environments

To accommodate the various design methodologies and design flows employed by the wide range of our customers user profiles such as system designers, algorithm designers, software coders and logic designers, we provide the appropriate design environment tailored to each user profile for design creation, design implementation and design verification.

The Xilinx ISE® Design Suite features a complete tool chain for the three domain-specific categories: embedded, DSP and logic/connectivity. To further enhance productivity and help customers better manage the complexity of their designs, the ISE Design Suite enables designers to target area, performance, or power by simply selecting a design goal in the setup. The Xilinx ISE Design Suite also integrates with a wide range of third-party electronic design automation (EDA) software offerings and point-tools.

Intellectual Property

Xilinx and various third parties offer hundreds of free and for-license IP components to meet timing parameters, including a host of widely used IP such as GigE, Ethernet, memory controllers, and PCIe®, as well as an abundance of domain-specific IP, such as embedded, DSP and connectivity, and market-specific IP.

Development Boards, Reference Designs, Kits and Configuration Products

In addition to the broad selection of legacy development boards presently offered, we have introduced a new unified board strategy that enables the creation of a standardized and coordinated set of base boards available both from Xilinx and our ecosystem partners, all utilizing the industry-standard extensions. Adopting this standard for all of our base boards enables the creation of a unified, scalable and extensible delivery mechanism for all Xilinx Targeted Design Platforms.

As a part of the Targeted Design Platform support strategy, Xilinx has also defined a new class of reference designs called the Targeted Reference Designs that offer a consistent, robust framework that is scalable for customer modification and supported throughout the product lifecycle.

We also offer comprehensive development kits including hardware, design tools, IP and reference designs that are designed to streamline and accelerate the development of domain-specific and market-specific applications.

Finally, Xilinx offers a range of configuration products including one-time programmable and in-system programmable storage devices to configure Xilinx FPGAs. These PROM (programmable read-only memory) products support all of our FPGA devices.

Third-Party Ecosystem

Xilinx and certain third parties have developed and continue to offer a robust ecosystem of IP, boards, tools, services, and support through the Xilinx alliance program. Xilinx is also moving forward with these third parties to make Targeted Design Platforms extensible through third-party tools, IP, software, boards, and design services, and leveraged in customer designs.

Global Services

Xilinx engineering services and our third-party alliance member services enhance the substantial benefits of the Targeted Design Platforms by allowing the customer to focus even more on their core competencies, realize additional time-to-market efficiencies and reduce their fixed engineering costs. These services provide customers with engineering resources to augment their design team and to provide expert design-specific advice. Xilinx tailors its engineering services to the needs of its customer, ranging from hands-on training to full design creation and implementation.

See information under the caption "Results of Operations — Net Revenues" in Item 7. "Management's Discussion and Analysis of Financial Condition and Results of Operations" for information about our revenues from our product families.

Research and Development

Our research and development (R&D) activities are primarily directed towards the design of new ICs, the development of new software design automation tools for hardware and embedded software, the design of logic IP cores, the adoption of advanced semiconductor manufacturing processes for ongoing cost reductions, performance and signal integrity improvements and the lowering of PLD power consumption. As a result of our R&D efforts, we have introduced a number of new products during the past several years including the Virtex-6, Virtex-5 and Spartan-6 families. Additionally, we have made enhancements to our IP core offerings and introduced new versions of our ISE Design Suite. We extended our collaboration with our foundry suppliers in the development of 65-nm, 45-nm and 40-nm complementary metal oxide semiconductor (CMOS) manufacturing technology and we were the first company in the PLD industry to ship 65-nm and 45-nm high-volume FPGA devices.

Our R&D challenge is to continue to develop new products that create cost-effective solutions for customers. In fiscal 2009, 2008 and 2007, our R&D expenses were $355.4 million, $358.1 million and $388.1 million, respectively. We believe technical leadership and innovation are essential to our future success and we are committed to maintaining a significant level of R&D investment.

Sales and Distribution

We sell our products to OEMs and to electronic components distributors who resell these products to OEMs or contract manufacturers.

We use dedicated global sales and marketing organizations as well as independent sales representatives to generate sales. In general, we focus our direct demand creation efforts on a limited number of key accounts with independent sales representatives often addressing those customers in defined territories. Distributors create

demand within the balance of our customer base. Distributors also provide vendor-managed inventory, value-added services and logistics for a wide range of our OEM customers.

Whether Xilinx, the independent sales representative, or the distributor identifies the sales opportunity, a local distributor will process and fulfill the majority of all customer orders. In such situations, distributors are the sellers of the products and as such they bear all legal and financial risks generally related to the sale of commercial goods, such as credit loss, inventory shrinkage and theft, as well as foreign currency fluctuations, but excluding indemnity and warranty liability.

In accordance with our distribution agreements and industry practice, we have granted the distributors the contractual right to return certain amounts of unsold product on a periodic basis and also receive price adjustments for unsold product in the case of a subsequent change in list prices. Revenue recognition on shipments to distributors worldwide is deferred until the products are sold to the distributors end customers.

Avnet, Inc. (Avnet) distributes the substantial majority of our products worldwide. No end customer accounted for more than 10% of our net revenues in fiscal 2009, 2008 or 2007. As of March 28, 2009 and March 29, 2008, Avnet accounted for 81% and 83% of the Company s total accounts receivable, respectively. Resale of product through Avnet accounted for 55%, 61% and 67% of the Company s worldwide net revenues in fiscal 2009, 2008 and 2007, respectively. We also use other regional distributors throughout the world. From time to time, we may add or terminate distributors in specific geographies, as we deem appropriate given the level of business, their performance and financial condition. We believe distributors provide a cost-effective means of reaching a broad range of customers while providing efficient logistics services. Since PLDs are standard products, they do not present many of the inventory risks to distributors posed by custom gate arrays, and they simplify the requirements for distributor technical support. See Note 2. Summary of Significant Accounting Policies and Concentrations of Risk to our consolidated financial statements, included in Item 8. Financial Statements and Supplementary Data, for information about concentrations of credit risk and Note 17. Segment Information for information about our revenues from external customers and domestic and international operations.

Backlog

As of March 28, 2009, our backlog from OEM customers and backlog from end customers reported by our distributors scheduled for delivery within the next three months was $162.0 million, compared to $202.0 million as of March 29, 2008. Orders from end customers to our distributors are subject to changes in delivery schedules or to cancellation without significant penalty. As a result, backlogs from both OEM customers and end customers reported by our distributors as of any particular period may not be a reliable indicator of revenue for any future period.

Wafer Fabrication

As a fabless semiconductor company, we do not manufacture wafers used for our IC products or PROMs. Rather, we purchase wafers from multiple foundries including United Microelectronics Corporation (UMC), Toshiba Corporation (Toshiba), Seiko Epson Corporation (Seiko), Samsung Electronics Co., Ltd. and He Jian Technology (Suzhou) Co., Ltd. Currently, UMC manufactures the substantial majority of our wafers. Precise terms with respect to the volume and timing of wafer production and the pricing of wafers produced by the semiconductor foundries are determined by our periodic negotiations with the wafer foundries.

Our strategy is to focus our resources on market development and creating new ICs and software design tools rather than on wafer fabrication. We continuously evaluate opportunities to enhance foundry relationships and/or obtain additional capacity from our main suppliers as well as other suppliers of leading-edge process technologies.

In September 1995, we entered into a joint venture with UMC and other parties to construct a wafer fabrication facility in Taiwan, known as United Silicon Inc. (USIC). In January 2000, as a result of the merger of USIC into UMC, our equity position in USIC was converted into shares of UMC, which are publicly traded on the Taiwan Stock Exchange. In fiscal 2007, we sold a portion of our UMC shares and we sold the remaining shares of our UMC investment in the fourth quarter of fiscal 2008.

In fiscal 1997, we signed a wafer purchasing agreement with Seiko. Seiko manufactures wafers for some of our most mature product lines.

In October 2004, the Company entered into an advanced purchase agreement with Toshiba under which the Company paid Toshiba a total of $100.0 million in two equal installments for advance payment of silicon wafers produced under the agreement. The original agreement was extended to December 2008. The balance of the advance payment remaining was zero as of March 28, 2009.

Sort, Assembly and Test

Wafers purchased are sorted by the foundry, independent sort subcontractors, or by Xilinx. Sorted die are assembled by subcontractors. During the assembly process, the wafers are separated into individual die, which are then assembled into various package types. Following assembly, the packaged units are tested by Xilinx personnel at our San Jose, California, Dublin, Ireland or Singapore facilities or by independent test subcontractors. We purchase most of our assembly and some of our testing services from Siliconware Precision Industries Ltd. in Taiwan, Amkor Technology, Inc. in Korea and the Philippines and STATS ChipPAC Ltd. in Singapore.

Quality Certification

Xilinx has achieved quality management systems certification for ISO 9001:2000 for our facilities in San Jose, California, Dublin, Ireland, Longmont, Colorado, Singapore and Albuquerque, New Mexico. In addition, Xilinx achieved ISO 14001, TL 9000 and TS 16949 environmental and quality certifications in the San Jose, Dublin and Singapore locations, TL 9000 certifications in the Longmont and Albuquerque locations and TS 16949 certifications in the Albuquerque and Hyderabad, India locations.

Patents and Licenses

While our various proprietary intellectual property rights are important to our success, we believe our business as a whole is not materially dependent on any particular patent or license, or any particular group of patents or licenses. As of March 28, 2009, we held more than 2,000 issued United States (U.S.) patents, which vary in duration, and over 750 pending U.S. patent applications relating to our proprietary technology. We maintain an active program of filing for additional patents in the areas of, but not limited to, circuits, software, IC architecture, system design, testing methodologies and other technologies relating to PLDs. We have licensed some parties to certain portions of our patent portfolio and obtained licenses to certain third-party patents as well.

We have acquired various licenses from third parties to certain technologies that are implemented in IP cores or embedded in our PLDs, such as processors. Those licenses support our continuing ability to make and sell these PLDs to our customers. We also sublicense certain third-party proprietary software and open-source software, such as compilers, for our design tools. Continued use of those software components is important to the operation of the design tools upon which customers depend.

We maintain the Xilinx trade name as well as numerous trademarks and registered trademarks including Xilinx, Virtex, Spartan, ISE, and associated logos. Maintaining these rights, and the goodwill associated with these trademarks and logos, is important to our business. We also have license rights to use certain trademarks owned by consortiums and other trademark owners that are related to our products and business.

We intend to protect our intellectual property vigorously. We believe that failure to enforce our intellectual property rights (including, for example, patents, copyrights and trademarks) or failure to protect our trade secrets effectively could have an adverse effect on our financial condition and results of operations. In the future, we may incur potentially significant litigation expenses to defend against claims of infringement or to enforce our intellectual property rights against third parties. However, any such litigation may or may not be successful.

Employees

As of March 28, 2009, we had 3,145 employees compared to 3,415 as of the end of the prior fiscal year. None of our employees are represented by a labor union. We have not experienced any work stoppages and believe we maintain good employee relations.

Competition

Our PLDs compete in the logic IC industry, an industry that is intensely competitive and characterized by rapid technological change, increasing levels of integration, product obsolescence and continuous price erosion. We expect increased competition from our primary PLD competitors, Altera Corporation (Altera), Lattice Semiconductor Corporation (Lattice) and Actel Corporation (Actel), from the ASIC market, which has been ongoing since the inception of FPGAs, from the ASSP market, and from new companies that may enter the traditional programmable logic market segment. Other competitors include manufacturers of:

- high-density programmable logic products characterized by FPGA-type architectures;
- high-volume and low-cost FPGAs as programmable replacements for ASICs and ASSPs;
- ASICs and ASSPs with incremental amounts of embedded programmable logic;
- high-speed, low-density CPLDs;
- high-performance DSP devices;
- products with embedded processors;
- products with embedded multi-gigabit transceivers; and
- other new or emerging programmable logic products.

We believe that important competitive factors in the logic IC industry include:

- product pricing;
- time-to-market;
- product performance, reliability, quality, power consumption and density;
- field upgradability;
- adaptability of products to specific applications;
- ease of use and functionality of software design tools;
- availability and functionality of predefined IP cores of logic;
- inventory management;
- access to leading-edge process technology and assembly capacity; and
- ability to provide timely customer service and support.

Our strategy for expansion in the logic market includes continued introduction of new product architectures that address high-volume, low-cost and low-power applications as well as high-performance, high-density applications. In addition, we anticipate continued price reductions proportionate with our ability to lower the cost for established products. We also recognize that different applications require different programmable technologies, and we are developing architectures, processes and products to meet these varying customer needs. To the extent that our efforts to compete are not successful, our financial condition and results of operations could be materially adversely affected.

Executive Officers of the Registrant

Certain information regarding the executive officers of Xilinx as of June 1, 2009 is set forth below:

Name	Age	Position
Moshe N. Gavrielov	54	President and Chief Executive Officer (CEO)
Scott R. Hover-Smoot	54	Vice President, General Counsel and Secretary
Jon A. Olson	55	Senior Vice President, Finance and Chief Financial Officer (CFO)
Victor Peng	49	Senior Vice President, Programmable Platforms Development
Raja G.	45	Senior Vice President, Worldwide Operations

Petrakian Vincent F. Ratford	57	Senior Vice President, Worldwide Marketing
Vincent L. Tong	47	Senior Vice President, Worldwide Quality and New Product Introductions
Frank A. Tornaghi	54	Senior Vice President, Worldwide Sales

There are no family relationships among the executive officers of the Company or the Board of Directors.

Moshe N. Gavrielov joined the Company in January 2008 as President and CEO and was appointed to the Board of Directors in February 2008. Prior to joining the Company, he served at Cadence Design Systems, Inc., an electronic design automation company, as Executive Vice President and General Manager of the Verification Division from April 2005 through November 2007. Mr. Gavrielov served as CEO of Verisity Ltd., an electronic design automation company, from March 1998 to April 2005 prior to its acquisition by Cadence Design Systems, Inc. Prior to joining Verisity, Mr. Gavrielov spent nearly 10 years at LSI Corporation (formerly LSI Logic Corporation), a semiconductor manufacturer, in a variety of executive management positions, including Executive Vice President of the Products Group, Senior Vice President and General Manager of International Marketing and Sales and Senior Vice President and General Manager of LSI Logic Europe plc. Prior to joining LSI Corporation, Mr. Gavrielov held various engineering and engineering management positions at Digital Equipment Corporation and National Semiconductor Corporation.

Scott R. Hover-Smoot joined the Company in October 2007 as Vice President, General Counsel and Secretary. From November 2001 to October 2007, Mr. Hover-Smoot served as Regional Counsel and Director of Legal Operations with Taiwan Semiconductor Manufacturing Company, Ltd., an independent semiconductor foundry. He served as Vice President and General Counsel of California Micro Devices Corporation, a provider of application-specific protection devices and display electronics devices from June

1994 to November 2001. Prior to joining California Micro Devices Corporation, Mr. Hover-Smoot spent over 20 years working in law firms including Berliner-Cohen, Flehr, Hohbach, Test, Albritton & Herbert, and Lyon & Lyon.

Jon A. Olson joined the Company in June 2005 as Vice President, Finance and CFO. Mr. Olson was promoted to his current position of Senior Vice President, Finance and CFO in August 2006. Prior to joining the Company, Mr. Olson spent more than 25 years at Intel Corporation, a semiconductor chip maker, serving in a variety of positions, including Vice President, Finance and Enterprise Services, Director of Finance.

Victor Peng joined the Company in April 2008 as Senior Vice President, Silicon Engineering Group and assumed his current position of Senior Vice President, Programmable Platforms Development in November 2008. Prior to joining the Company, Mr. Peng served as Corporate Vice President, Graphics Products Group at Advanced Micro Devices (AMD), a provider of processing solutions, from November 2005 to April 2008. Before joining AMD, Mr. Peng served as Vice President of Silicon Engineering in the Graphics Products Group business unit at ATI Technologies, a graphics processor unit provider, from April 2005 until its acquisition by AMD. Before joining ATI Technologies, Mr. Peng served as Vice President of Engineering at TZero Technologies, a fabless semiconductor company, from September 2004 to April 2005. From November 2000 to September 2004, Mr. Peng served as Vice President of Engineering at MIPS Technologies, a semiconductor design IP company.

Raja G. Petrakian joined the Company in October 1995 and has served in a number of key roles within Operations, most recently as Senior Director of Supply Chain Management and Vice President of Supply Chain Management. Dr. Petrakian was promoted to his current position of Senior Vice President, Worldwide Operations in March 2009. Prior to joining Xilinx, Dr. Petrakian spent more than three years at the IBM T.J. Research Center serving as a research staff member in the Manufacturing Research Department.

Vincent F. Ratford joined the Company in January 2006 as Vice President of Marketing, Business Development and Silicon Architecture. Mr. Ratford was promoted to Vice President and General Manager in October 2007. He was promoted to Senior Vice President, Solutions Development Group in April 2008 and assumed his current position of Senior Vice President, Worldwide Marketing in November 2008. Prior to joining the Company, he served as President and CEO of AccelChip, Inc. (AccelChip), a provider of synthesis software tools for designing DSP systems, from July 2004 until its acquisition by Xilinx in January 2006. Prior to that, Mr. Ratford operated the consulting firm, DeepTech Consulting, from April 2002 to July 2004. Mr. Ratford worked at Virage Logic Corporation, a provider of semiconductor IP, as Vice President of Marketing and Business Development from July 2000 to April 2002 and as Vice President of Sales and Marketing from February 1998 to July 2000. Before joining Virage Logic, Mr. Ratford served as Chief Operating Officer of the Microtec Division of Mentor Graphics, a provider of hardware and software design solutions to semiconductor companies, from October 1995 to December 1997. Before joining the Microtec Division, he was Director of Marketing for Mentor Graphics System Design Division from May 1993 to October 1995.

Vincent L. Tong joined the Company in May 1990 and has served in a number of key roles, most recently as Vice President of Product Technology and as Vice President, Worldwide Quality and Reliability. In April 2008, he was promoted to his current position of Senior Vice President, Worldwide Quality and New Product Introductions. Prior to joining the Company, Mr. Tong served in a variety of engineering positions at Monolithic Memories, a producer of logic devices, and AMD. Mr. Tong serves on the board of the Global Semiconductor Alliance, a non-profit semiconductor organization.

Frank A. Tornaghi joined the Company in February 2008 as Vice President, Worldwide Sales and was promoted to his current position of Senior Vice President, Worldwide Sales in April 2008. Prior to joining the Company, Mr. Tornaghi spent 22 years at LSI Corporation. Mr. Tornaghi acted as an independent consultant from April 2006 until he joined the Company. He served as Executive Vice President, Worldwide Sales at LSI Corporation from July 2001 to April 2006 and as Vice President, North America Sales, from May 1993 to July 2001. From 1984 until May 1993, Mr. Tornaghi held various management positions in sales at LSI Corporation.

Additional Information

Our Internet address is www.xilinx.com. We make available, via a link through our investor relations website located at www.investor.xilinx.com, access to our Annual Report on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K and any amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the U.S. Securities Exchange Act of 1934, as amended (Exchange Act) as soon as reasonably practicable after they are electronically filed with or furnished to the Securities and Exchange Commission (SEC). All such filings on our investor relations website are available free of charge. Printed copies of these documents are also available to stockholders without charge, upon written request directed to Xilinx, Inc., Attn: Investor Relations, 2100 Logic Drive, San Jose, CA 95124. Further, a copy of this Annual Report on Form 10-K is located at the SEC s Public Reference Room at 100 F Street, N.E., Room 1580, Washington, D.C. 20549. Information on the operation of the Public Reference Room can be obtained by calling the SEC at 1-800-SEC-0330. The SEC maintains an Internet site that contains reports, proxy and information statements and other information regarding our filings at http://www.sec.gov. The content on any website referred to in this filing is not incorporated by reference into this filing unless expressly noted otherwise.

Additional information required by this Item 1 is incorporated by reference to the section captioned Net Revenues Net Revenues by Geography in Item 7. Management s Discussion and Analysis of Financial Condition and Results of Operations and to Note 17. Segment Information to our consolidated financial statements, included in Item 8. Financial Statements and Supplementary Data.

This annual report includes trademarks and service marks of Xilinx and other companies that are unregistered and registered in the United States and other countries.

ITEM 1A. RISK FACTORS

The following risk factors and other information included in this Annual Report on Form 10-K should be carefully considered. The risks and uncertainties described below are not the only risks to the Company. Additional risks and uncertainties not presently known to the Company or that the Company s management currently deems immaterial also may impair its business operations. If any of the risks described below were to occur, our

business, financial condition, operating results and cash flows could be materially adversely affected.

General economic conditions and the related deterioration in the global business environment could have a material adverse effect on our business, operating results and financial condition.

Global consumer confidence has eroded amidst concerns over declining asset values, inflation, volatility in energy costs, geopolitical issues, the availability and cost of credit, rising unemployment, and the stability and solvency of financial institutions, financial markets, businesses and sovereign nations, among other concerns. These concerns have slowed global economic growth and have resulted in recessions in numerous countries, including many of those in North America, Europe and Asia. Recent economic conditions had a negative impact on our results of operations during the third and fourth quarters of fiscal 2009 due to reduced customer demand and it is unclear when economic conditions will improve. As these economic conditions continue to persist, or if they worsen, a number of negative effects on our business could result, including customers or potential customers reducing or delaying orders, the insolvency of key suppliers, which could result in production delays, the inability of customers to obtain credit, and the insolvency of one or more customers. Any of these effects could impact our ability to effectively manage inventory levels and collect receivables and ultimately decrease our net revenues and profitability.

The semiconductor industry is characterized by cyclical market patterns and a significant industry downturn could adversely affect our operating results.

The semiconductor industry is highly cyclical and our financial performance has been affected by downturns in the industry, including the current downturn. Down cycles are generally characterized by price erosion and weaker demand for our products. Weaker demand for our products resulting from economic conditions in the end markets we serve and reduced capital spending by our customers can result, and in the past has resulted in excess and obsolete inventories and corresponding inventory write-downs. We attempt to identify changes in market conditions as soon as possible; however, the dynamics of the market make prediction of and timely reaction to such events difficult. Due to these and other factors, our past results are much less reliable predictors of the future than for companies in older, more stable industries.

The nature of our business makes our revenues difficult to predict which could have an adverse impact on our business.

In addition to the challenging market conditions we may face, we have limited visibility into the demand for our products, particularly new products, because demand for our products depends upon our products being designed into our end customers products and those products achieving market acceptance. Due to the complexity of our customers designs, the design to volume production process for our customers requires a substantial amount of time, frequently longer than a year. In addition, we are increasingly dependent upon turns, orders received and turned for shipment in the same quarter, and we have historically derived a significant portion of our quarterly revenue during the last weeks of the quarter. These factors make it difficult for us to forecast future sales and project quarterly revenues. The difficulty in forecasting future sales impairs our ability to project our inventory requirements, which could result, and in the past has resulted in inventory write-downs or failure to timely meet customer product demands. In addition, difficulty in forecasting revenues compromises our ability to provide forward-looking revenue and earnings guidance.

Global economic conditions, the economic conditions of the countries in which we operate and currency fluctuations could have a material adverse affect on our business and negatively impact our financial condition and results of operations.

In addition to our U.S. operations, we also have significant international operations, including foreign sales offices to support our international customers and distributors, our regional headquarters in Ireland and Singapore and a research and development site in India. In connection with the restructuring we announced in April 2009, we expect our international operations to grow as we relocate certain operations and administrative functions. Sales and operations outside of the U.S. subject us to the risks associated with conducting business in foreign economic and regulatory environments. Our financial condition and results of operations could be adversely affected by unfavorable economic conditions in countries in which we do significant business or by changes in foreign currency exchange rates affecting those countries. The Company derives over one-half of its revenues from international sales,

primarily in the Asia Pacific region, Europe and Japan. Past and current economic weakness in these markets adversely affected revenues. The timing and nature of economic recovery in these markets as well as in the U.S. remains uncertain, and there can be no assurance that global market conditions will improve in the near future. Sales to all direct OEMs and distributors are denominated in U.S. dollars. While the recent movement of the Euro and Yen against the U.S. dollar had no material impact to our business, increased volatility could impact our European and Japanese customers. Currency instability and recent volatility and disruptions in the credit and capital markets may increase credit risks for some of our customers and may impair our customers' ability to repay existing obligations. Increased currency volatility could also positively or negatively impact our foreign-currency-denominated costs, assets and liabilities. In addition, devaluation of the U.S. dollar relative to other foreign currencies may increase the operating expenses of our foreign subsidiaries adversely affecting our results of operations. Furthermore, because we are increasingly dependent on the global economy, instability in worldwide economic environments occasioned, for example, by political instability, terrorist activity or U.S. military actions could impact economic activity and lead to a contraction of capital spending by our customers. Any or all of these factors could adversely affect our financial condition and results of operations in the future.

We are exposed to fluctuations in interest rates and changes in credit rating and in the market values of our portfolio investments which could have a material adverse impact on our financial condition and results of operations.

Our cash, short-term and long-term investments represent significant assets that may be subject to fluctuating or even negative returns depending upon interest rate movements, changes in credit rating and financial market conditions. Since September 2007, the global credit markets have experienced adverse conditions that have negatively impacted the values of various types of investment and non-investment grade securities. The global credit and capital markets have recently experienced further significant volatility and disruption due to instability in the global financial system and the current uncertainty related to global economic conditions. As of March 28, 2009, less than 7% of our $1.58 billion investment portfolio consisted of asset-backed securities and approximately 11% of the portfolio consisted of mortgage-backed securities. Asset-backed securities consisted of student loan auction rate securities and other asset-backed securities.

Approximately 4% of our investment portfolio consisted of student loan auction rate securities and all of these securities are rated AAA with the exception of approximately 14% that were downgraded to A rating during the fourth quarter of fiscal 2009. More than 98% of the underlying assets that secure the student loan auction rate securities are pools of student loans originated under the Federal Family Education Loan Program (FFELP) that are substantially guaranteed by the U.S. Department of Education. These securities experienced failed auctions in the fourth quarter of fiscal 2008 due to liquidity issues in the global credit markets. In a failed auction, the interest rates are reset to a maximum rate defined by the contractual terms for each security. We have collected and expect to collect all interest payable on these securities when due. During fiscal 2009, $1.4 million of these student loan auction rate securities were redeemed for cash by the issuers at par value. Beginning with the quarter ended March 29, 2008, the student loan auction rate securities were reclassified from short-term to long-term investments on the consolidated balance sheets since there can be no assurance of a successful auction in the future. The final maturity dates range from March 2023 to November 2047.

All other asset-backed securities comprised less than 3% of our investment portfolio as of March 28, 2009, of which approximately 9% are AAA rated with the majority of the rest of the asset-backed securities rated A or BBB. These asset-backed securities are secured primarily by bank, finance and insurance company obligations, collateralized loan and bank obligations, credit card debt and mortgage-backed securities with no direct U.S. subprime mortgage exposure. Substantially all of the other mortgage-backed securities in the investment portfolio are AAA rated, were issued by U.S. government-sponsored enterprises and agencies and represented approximately 11% of the investment portfolio as of March 28, 2009. As a result of these recent adverse conditions in the global credit markets, there is a risk that we may incur additional other-than-temporary impairment charges for certain types of investments such as asset-backed securities should the credit markets experience further deterioration or the underlying assets fail to perform as anticipated due to the continued or worsening global economic conditions. Our future investment income may fall short of expectations due to changes in interest rates or if the decline in fair values of our debt securities is judged to be other than temporary. Furthermore, we may suffer losses in principal if we are forced to sell securities that have declined in market value due to changes in interest rates or financial market conditions. See "Note 4. Financial Instruments" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data," for a table of our available-for-sale securities.

We are subject to the risks associated with conducting business operations outside of the U.S. which could adversely affect our business.

In addition to international sales and support operations and development activities, we purchase our wafers from foreign foundries and have our commercial products assembled, packaged and tested by subcontractors located outside the U.S. In connection with the restructuring we announced in April 2009, we expect these subcontractor activities to increase. All of these activities are subject to the uncertainties associated with international business operations, including tax laws and regulations, trade barriers, economic sanctions, import and export regulations, duties and tariffs and other trade restrictions, changes in trade policies, foreign governmental regulations, reduced protection for IP, longer receivable collection periods and disruptions or delays in production or shipments, any of which could have a material adverse effect on our business, financial condition and/or operating results. Additional factors that could adversely affect us due to our international operations include rising oil prices and increased costs of natural resources. Moreover, our financial condition and results of operations could be affected in the event of political conflicts or economic crises in

countries where our main wafer providers, end customers and contract manufacturers who provide assembly and test services worldwide, are located. Adverse change to the circumstances or conditions of our international business operations could have a material adverse effect on our business.

Our success depends on our ability to develop and introduce new products and failure to do so would have a material adverse impact on our financial condition and results of operations.

Our success depends in large part on our ability to develop and introduce new products that address customer requirements and compete effectively on the basis of price, density, functionality, power consumption and performance. The success of new product introductions is dependent upon several factors, including:

- timely completion of new product designs;
- ability to generate new design opportunities or "design wins";
- availability of specialized field application engineering resources supporting demand creation and customer adoption of new products;
- ability to utilize advanced manufacturing process technologies on circuit geometries of 65nm and smaller;
- achieving acceptable yields;
- ability to obtain adequate production capacity from our wafer foundries and assembly and test subcontractors;
- ability to obtain advanced packaging;
- availability of supporting software design tools;
- utilization of predefined IP cores of logic;
- customer acceptance of advanced features in our new products; and
- market acceptance of our customers' products.

Our product development efforts may not be successful, our new products may not achieve industry acceptance and we may not achieve the necessary volume of production that would lead to further per unit cost reductions. Revenues relating to our mature products are expected to decline in the future, which is normal for our product life cycles. As a result, we may be increasingly dependent on revenues derived from design wins for our newer products as well as anticipated cost reductions in the manufacture of our current products. We rely primarily on obtaining yield improvements and corresponding cost reductions in the manufacture of existing products and on introducing new products that incorporate advanced features and other price/performance factors that enable us to increase revenues while maintaining consistent margins. To the extent that such cost reductions and new product introductions do not occur in a timely manner, or to the extent that our products do not achieve market acceptance at prices with higher margins, our financial condition and results of operations could be materially adversely affected.

We are dependent on independent foundries for the manufacture of all of our products and a manufacturing problem or insufficient foundry capacity could adversely affect our operations.

During fiscal 2009, nearly all of our wafers were manufactured either in Taiwan, by UMC or in Japan, by Toshiba or Seiko. Terms with respect to the volume and timing of wafer production and the pricing of wafers produced by the semiconductor foundries are determined by periodic negotiations between Xilinx and these wafer foundries,

which usually result in short-term agreements that do not provide for long-term supply or allocation commitments. We are dependent on these foundries, especially UMC, which supplies the substantial majority of our wafers. We rely on UMC to produce wafers with competitive performance and cost attributes. These attributes include an ability to transition to advanced manufacturing process technologies and increased wafer sizes, produce wafers at acceptable yields and deliver them in a timely manner. We cannot guarantee that the foundries that supply our wafers will not experience manufacturing problems, including delays in the realization of advanced manufacturing process technologies or difficulties due to limitations of new and existing process technologies. Furthermore, we cannot guarantee the foundries will be able to manufacture sufficient quantities of our products. In addition, current economic conditions may adversely impact the financial health and viability of the foundries and result in their insolvency or their inability to meet their commitments to us. The insolvency of a foundry or any significant manufacturing problem or insufficient foundry capacity would disrupt our operations and negatively impact our financial condition and results of operations.

We have established other sources of wafer supply for our products in an effort to secure a continued supply of wafers. However, establishing, maintaining and managing multiple foundry relationships requires the investment of management resources as well as additional costs. If we do not manage these relationships effectively, it could adversely affect our results of operations.

Increased costs of wafers and materials, or shortages in wafers and materials, could adversely impact our gross margins and lead to reduced revenues.

If greater demand for wafers produced by the foundries is not offset by an increase in foundry capacity, or market demand for wafers or production and assembly materials increases, our supply of wafers and other materials could become limited. Such shortages raise the likelihood of potential wafer price increases and wafer shortages or shortages in materials at production and test facilities. Such

increases in wafer prices or materials could adversely affect our gross margins and shortages of wafers and materials would adversely affect our ability to meet customer demands.

Earthquakes and other natural disasters could disrupt our operations and have a material adverse affect on our financial condition and results of operations.

The independent foundries, upon which we rely to manufacture our products, as well as our California and Singapore facilities, are located in regions that are subject to earthquakes and other natural disasters. UMC's foundries in Taiwan and Toshiba's and Seiko's foundries in Japan as well as many of our operations in California are centered in areas that have been seismically active in the recent past and some areas have been affected by other natural disasters. Any catastrophic event in these locations will disrupt our operations, including our manufacturing activities. This type of disruption could result in our inability to manufacture or ship products, thereby materially adversely affecting our financial condition and results of operations. Additionally, disruption of operations at these foundries for any reason, including other natural disasters such as typhoons, fires or floods, as well as disruptions in access to adequate supplies of electricity, natural gas or water could cause delays in shipments of our products, and could have a material adverse effect on our results of operations.

We are dependent on independent subcontractors for most of our assembly and test services and unavailability or disruption of these services could negatively impact our financial condition and results of operations.

We are also dependent on subcontractors to provide semiconductor assembly, substrate, test and shipment services. Any prolonged inability to obtain wafers with competitive performance and cost attributes, adequate yields or timely delivery, any disruption in assembly, test or shipment services, or any other circumstance that would require us to seek alternative sources of supply, could delay shipments and have a material adverse effect on our ability to meet customer demands. In addition, current economic conditions may adversely impact the financial health and viability of these subcontractors and result in their insolvency or their inability to meet their commitments to us. These factors would result in reduced net revenues and could negatively impact our financial condition and results of operations.

If we are not able to successfully compete in our industry, our financial results and future prospects will be adversely affected.

Our PLDs compete in the logic IC industry, an industry that is intensely competitive and characterized by rapid technological change, increasing levels of integration, product obsolescence and continuous price erosion. We expect increased competition from our primary PLD competitors, Altera, Lattice and Actel, from the ASIC market, which has been ongoing since the inception of FPGAs, from the ASSP market, and from new companies that may enter the traditional programmable logic market segment. We believe that important competitive factors in the logic IC industry include:

- product pricing;
- time-to-market;
- product performance, reliability, quality, power consumption and density;
- field upgradability;
- adaptability of products to specific applications;
- ease of use and functionality of software design tools;
- availability and functionality of predefined IP cores of logic;
- inventory management;
- access to leading-edge process technology and assembly capacity; and
- ability to provide timely customer service and support.

Our strategy for expansion in the logic market includes continued introduction of new product architectures that address high-volume, low-cost and low-power applications as well as high-performance, high-density applications. In addition, we anticipate continued price reductions proportionate with our ability to lower the cost for established products. However, we may not be successful in achieving these strategies.

Other competitors include manufacturers of:

- high-density programmable logic products characterized by FPGA-type architectures;
- high-volume and low-cost FPGAs as programmable replacements for ASICs and ASSPs;
- ASICs and ASSPs with incremental amounts of embedded programmable logic;
- high-speed, low-density CPLDs;
- high-performance DSP devices;
- products with embedded processors;
- products with embedded multi-gigabit transceivers; and
- other new or emerging programmable logic products.

Several companies have introduced products that compete with ours or have announced their intention to sell PLD products. To the extent that our efforts to compete are not successful, our financial condition and results of operations could be materially adversely affected.

The benefits of programmable logic have attracted a number of competitors to this segment. We recognize that different applications require different programmable technologies, and we are developing architectures, processes and products to meet these varying customer needs. Recognizing the increasing importance of standard software solutions, we have developed common software design tools that support the full range of our IC products. We believe that automation and ease of design are significant competitive factors in this segment.

We could also face competition from our licensees. In the past we have granted limited rights to other companies with respect to certain of our older technology, and we may do so in the future. Granting such rights may enable these companies to manufacture and market products that may be competitive with some of our older products.

Our failure to protect and defend our intellectual property could impair our ability to compete effectively.

We rely upon patent, copyright, trade secret, mask work and trademark laws to protect our intellectual property. We cannot provide assurance that such intellectual property rights can be successfully asserted in the future or will not be invalidated, circumvented or challenged. From time to time, third parties, including our competitors, have asserted against us patent, copyright and other intellectual property rights to technologies that are important to us. Third parties may assert infringement claims against our indemnitees or us in the future. Assertions by third parties may result in costly litigation or indemnity claims and we may not prevail in such matters or be able to license any valid and infringed patents from third parties on commercially reasonable

terms. This could result in the loss of our ability to import and sell our products. Any infringement claim, indemnification claim, or impairment or loss of use of our intellectual property could materially adversely affect our financial condition and results of operations.

We rely on information technology systems, and failure of these systems to function properly could result in business disruption.

We rely in part on various information technology (IT) systems to manage our operations, including financial reporting, and we regularly evaluate these systems and make changes to improve them as necessary. Consequently, we periodically implement new, or enhance existing, operational and IT systems, procedures and controls. For example, we recently simplified our supply chain and were required to make certain changes to our IT systems. Any delay in the implementation of, or disruption in the transition to, new or enhanced systems, procedures or controls, could harm our ability to record and report financial and management information on a timely and accurate basis. Further, these systems are subject to power and telecommunication outages or other general system failure. Failure of our IT systems or difficulties in managing them could result in business disruption.

If we are unable to maintain effective internal controls, our stock price could be adversely affected.

We are subject to the ongoing internal control provisions of Section 404 of the Sarbanes-Oxley Act of 2002 (the Act). Our controls necessary for continued compliance with the Act may not operate effectively at all times and may result in a material weakness disclosure. The identification of material weaknesses in internal control, if any, could indicate a lack of proper controls to generate accurate financial statements and could cause investors to lose confidence and our stock price to drop. Further, our internal control effectiveness may be impacted upon executing the restructuring plan announced in April 2009 if we are unable to successfully transfer certain control activities and responsibilities to new personnel in different locations.

Unfavorable results of legal proceedings could adversely affect our financial condition and operating results.

From time to time we are subject to various legal proceedings and claims that arise out of the ordinary conduct of our business. Certain claims are not yet resolved, including those that are discussed in Item 3. Legal Proceedings, included in Part I, and additional claims may arise in the future. Results of legal proceedings cannot be predicted with certainty. Regardless of its merit, litigation may be both time-consuming and disruptive to our operations and cause significant expense and diversion of management attention and we may enter into material settlements to avoid these risks. Should the Company fail to prevail in certain matters, or should several of these matters be resolved against us in the same reporting period, we may be faced with significant monetary damages or injunctive relief against us that would materially and adversely affect a portion of our business and might materially and adversely affect our financial condition and operating results.

Our products could have defects which could result in reduced revenues and claims against us.

We develop complex and evolving products that include both hardware and software. Despite our testing efforts and those of our subcontractors, defects may be found in existing or new products. These defects may cause us to incur significant warranty, support and repair or replacement costs, divert the attention of our engineering personnel from our product development efforts and harm our

relationships with customers. Product defects or other performance problems could result in the delay or loss of market acceptance of our products and would likely harm our business. Our customers could also seek damages from us for their losses. A product liability claim brought against us, even if unsuccessful, would likely be time-consuming and costly to defend. Product liability risks are particularly significant with respect to aerospace, automotive and medical applications because of the risk of serious harm to users of these products. Any product liability claim, whether or not determined in our favor, could result in significant expense, divert the efforts of our technical and management personnel, and harm our business.

In preparing our financial statements, we make good faith estimates and judgments that may change or turn out to be erroneous.

In preparing our financial statements in conformity with accounting principles generally accepted in the United States, we must make estimates and judgments in applying our most critical accounting policies. Those estimates and judgments have a significant impact on the results we report in our consolidated financial statements. The most difficult estimates and subjective judgments that we make concern valuation of marketable and non-marketable securities, revenue recognition, inventories, long-lived assets, taxes, legal matters and stock-based compensation. We base our estimates on historical experience and on various other assumptions that we believe to be reasonable under the circumstances, the results of which form the basis for making judgments about the carrying values of assets and liabilities that are not readily apparent from other sources. We also have other key accounting policies that are not as subjective, and therefore, their application would not require us to make estimates or judgments that are as difficult, but which nevertheless could significantly affect our financial reporting. Actual results may differ materially from these estimates. If these estimates or their related assumptions change, our operating results for the periods in which we revise our estimates or assumptions could be adversely and perhaps materially affected.

We depend on distributors, primarily Avnet, to generate a majority of our sales and complete order fulfillment.

Resale of product through Avnet accounted for 55% of the Company□s worldwide net revenues in fiscal 2009 and as of March 28, 2009, Avnet accounted for 81% of our total accounts receivable. In addition, we are subject to concentrations of credit risk in our trade accounts receivable, which includes accounts of our distributors. A significant reduction of effort by a distributor to sell our products or a material change in our relationship with one or more distributors may reduce our access to certain end customers and adversely affect our ability to sell our products. Furthermore, if a key distributor materially defaults on a contract or otherwise fails to perform, our business and financial results would suffer.

In addition, the financial health of our distributors and our continuing relationships with them are important to our success. Current economic conditions may adversely impact the financial health of some of these distributors, particularly our smaller distributors. This could result in the insolvency of certain distributors, the inability of distributors to obtain credit to finance the purchase of our products, or cause distributors to delay payment of their obligations to us and increase our credit risk exposure. Our business could be harmed if the financial health of these distributors impairs their performance and we are unable to secure alternate distributors.

Reductions in the average selling prices of our products could have a negative impact on our gross margins.

The average selling prices of our products generally decline as the products mature. We seek to offset the decrease in selling prices through yield improvement, manufacturing cost reductions and increased unit sales. We also continue to develop higher value products or product features that increase, or slow the decline of, the average selling price of our products. However, there is no guarantee that our ongoing efforts will be successful or that they will keep pace with the decline in selling prices of our products, which could ultimately lead to a decline in revenues and have a negative effect on our gross margins.

A number of factors can impact our gross margins.

A number of factors, including our product mix, market acceptance of our new products, competitive pricing dynamics, geographic and/or market segment pricing strategies and various manufacturing cost variables cause our gross margins to fluctuate. In addition, forecasting our gross margins is difficult because the majority of our business is based on turns within the same quarter.

If we do not successfully implement the restructuring we announced in April 2009, our results of operations and financial condition could be adversely impacted.

In April 2009, we announced restructuring measures and a net reduction in our global workforce by up to 200 positions, which we expect to complete by the fourth quarter of fiscal 2010. The positions will be eliminated across a variety of functions and geographies worldwide. The restructuring is designed to drive structural operating efficiencies across the Company and will align our Company with the evolving geographic distribution of our customers and supply chain. However, if we do not successfully implement this restructuring, our results of operations and financial condition could be adversely impacted. Factors that could cause actual results to differ materially from our expectations with regard to our announced restructuring include:

- the availability and hiring of the appropriately skilled workers in the Asia Pacific region;
- the transition of testing and other operational matters to third parties; and/or
- the timing and execution of our programs and plans related to the restructuring.

Considerable amounts of our common shares are available for issuance under our equity incentive plans and debentures, and significant issuances in the future may adversely impact the market price of our common shares.

As of March 28, 2009, we had 2.00 billion authorized common shares, of which 275.5 million shares were outstanding. In addition, 62.7 million common shares were reserved for issuance pursuant to our equity incentive plans and 1990 Employee Qualified Stock Purchase Plan (Employee Stock Purchase Plan), and 22.4 million shares were reserved for issuance upon conversion or repurchase of the 3.125% convertible debentures due March 15, 2037 (debentures). The availability of substantial amounts of our common shares resulting from the exercise or settlement of equity awards outstanding under our equity incentive plans or the conversion or repurchase of debentures using common shares, which would be dilutive to existing stockholders, could adversely affect the prevailing market price of our common shares and could impair our ability to raise additional capital through the sale of equity securities.

ITEM 1B. UNRESOLVED STAFF COMMENTS

Not applicable.

ITEM 2. PROPERTIES

Our corporate offices, which include the administrative, sales, customer support, marketing, R&D and manufacturing and testing groups, are located in San Jose, California. This main site consists of adjacent buildings providing 588,000 square feet of space, which we own. We also own two parcels of land totaling approximately 121 acres in South San Jose near our corporate facility. At present, we do not have any plans to develop the land. We also have a 106,000 square foot leased facility in San Jose, which we do not occupy and is presently listed for subleasing.

We also own a 228,000 square foot facility in the metropolitan area of Dublin, Ireland, which serves as our regional headquarters in Europe. The Irish facility is primarily used for manufacturing and testing of our products, service and support for our customers in Europe, R&D and IT support.

In addition, we also own a 222,000 square foot facility in Singapore, which serves as our Asia Pacific regional headquarters. We own the building but the land is subject to a 30-year lease expiring in November 2035. The Singapore facility is primarily used for manufacturing and testing of our products, service and support for our customers in Asia Pacific/Japan, coordination and management of certain third parties in our supply chain and R&D. Excess space in the facility is leased to tenants under long-term lease agreements.

We also own a 130,000 square foot facility in Longmont, Colorado. The Longmont facility serves as the primary location for our software efforts in the areas of R&D, manufacturing and quality control. In addition, we also own a 200,000 square foot facility and 40 acres of land adjacent to the Longmont facility for future expansion. The facility is partially leased to tenants under long-term lease agreements and partially used by the Company.

We own a 45,000 square foot facility in Albuquerque, New Mexico, which is used for the development of our CoolRunner CPLD product families as well as IP cores.

We lease office facilities for our engineering design centers in Portland, Oregon, Grenoble, France, Edinburgh, Scotland, Hyderabad, India and Toronto, Canada. We also lease sales offices in various locations throughout North America, which include the metropolitan areas of Chicago, Dallas, Los Angeles, Nashua, Ottawa, Raleigh, San Diego and Toronto as well as international sales offices located in the metropolitan areas of Beijing, Brussels, Helsinki, Hong Kong, London, Milan, Munich, Osaka, Paris, Seoul, Shanghai, Shenzhen, Stockholm, Taipei, Tel Aviv and Tokyo.

ITEM 3. LEGAL PROCEEDINGS

Internal Revenue Service

The Internal Revenue Service (IRS) audited and issued proposed adjustments to the Company's tax returns for fiscal 1996 through 2001. The Company filed petitions with the Tax Court in response to assertions by the IRS relating to fiscal 1996 through 2000. To date, all issues have been settled with the IRS in this matter except as described in the following paragraphs.

On August 30, 2005, the Tax Court issued its opinion concerning whether the value of stock options must be included in the cost sharing agreement with Xilinx Ireland. The Tax Court agreed with the Company that no amount for stock options was to be included in the cost sharing agreement, and thus, the Company had no tax, interest, or penalties due for this issue. The Tax Court entered its decision on May 31, 2006. On August 25, 2006, the IRS appealed the decision to the U.S. Court of Appeals for the Ninth Circuit.

The Company and the IRS presented oral arguments to a three-judge panel of the Appeals Court on March 12, 2008. On May 27, 2009, the Company received a 2-1 adverse judicial ruling from the Appeals Court reversing the Tax Court decision and holding that the Company should include stock option amounts in its cost sharing agreement with Xilinx Ireland. The Company does not agree with the Appeals Court decision and is reviewing its alternatives as a result of the decision.

The Company expects to record expense of $8.6 million in the first quarter of fiscal 2010 in order to reverse the interest income it accrued through March 28, 2009 on the earlier prepayment it made to the IRS. The Company is presently determining the amount of penalties and interest to be accrued under Financial Accounting Standards Board (FASB) Interpretation No. 48, "Accounting for Uncertainty in Income Taxes - an interpretation of FASB Statement No. 109" (FIN 48) in the first quarter of fiscal 2010 as a result of this decision.

In a separate matter, on December 8, 2008, the IRS issued a statutory notice of deficiency reflecting proposed audit adjustments for fiscal 2005. The Company filed a petition with the Tax Court on March 2, 2009, in response to this notice of deficiency and plans to contest the proposed adjustments. The Company believes it has provided adequate reserves for any tax deficiencies that could result from this IRS action.

Patent Litigation

On December 28, 2007, a patent infringement lawsuit was filed by PACT XPP Technologies, AG (PACT) against the Company in the U.S. District Court for the Eastern District of Texas, Marshall Division (PACT XPP Technologies, AG. v. Xilinx, Inc. and Avnet, Inc. Case No. 2:07-CV-563). The lawsuit pertains to 11 different patents and PACT seeks injunctive relief, unspecified damages and interest and attorneys' fees. Neither the likelihood, nor the amount of any potential exposure to the Company is estimable at this time.

On August 21, 2007, Lonestar Inventions, L.P. (Lonestar) filed a patent infringement lawsuit against Xilinx in the U.S. District Court for the Eastern District of Texas, Tyler Division (Lonestar Inventions, L.P. v. Xilinx, Inc. Case No. 6:07-CV-393). The lawsuit pertained to a single patent and Lonestar sought injunctive relief, unspecified damages and interest and attorneys' fees. The parties reached a confidential agreement to settle the action and the lawsuit was dismissed with prejudice on December 18, 2008. The amount of the settlement did not have a material impact on the Company's financial position or results of operations.

Other Matters

From time to time, we are involved in various disputes and litigation matters that arise in the ordinary course of our business. These include disputes and lawsuits related to intellectual property, mergers and acquisitions, licensing, contract law, tax, regulatory, distribution arrangements, employee relations and other matters. Periodically, we review the status of each matter and assess its potential financial exposure. If the potential loss from any claim or legal proceeding is considered probable and a range of possible losses can be estimated, we accrue a liability for the estimated loss. Legal proceedings are subject to uncertainties, and the outcomes are difficult to predict. Because of such uncertainties, accruals are based only on the best information available at the time. As additional information becomes available, we continue to reassess the potential liability related to

pending claims and litigation and may revise estimates.

ITEM 4. SUBMISSION OF MATTERS TO A VOTE OF SECURITY HOLDERS

No matters were submitted to a vote of security holders during the fourth quarter of the fiscal year covered by this report.

PART II

ITEM 5. MARKET FOR REGISTRANT'S COMMON EQUITY, RELATED STOCKHOLDER MATTERS AND ISSUER PURCHASES OF EQUITY SECURITIES

Our common stock trades on the NASDAQ Global Select Market under the symbol XLNX. As of May 6, 2009, there were approximately 793 stockholders of record. Since many holders shares are listed under their brokerage firms names, the actual number of stockholders is estimated by the Company to be over 105,000.

The following table sets forth the high and low closing sale prices, for the periods indicated, for our common stock as reported by the NASDAQ Global Select Market:

	Fiscal 2009		Fiscal 2008	
	High	Low	High	Low
First Quarter	$28.16	$22.96	$30.18	$25.65
Second Quarter	27.55	22.48	28.70	24.34
Third Quarter	23.45	14.61	26.97	21.16
Fourth Quarter	20.38	15.47	24.94	19.06

Dividends Declared Per Common Share

The following table presents the quarterly dividends declared on our common stock for the periods indicated:

	Fiscal 2009	Fiscal 2008
First Quarter	$0.14	$0.12
Second Quarter	0.14	0.12
Third Quarter	0.14	0.12
Fourth Quarter	0.14	0.12

On April 21, 2009, our Board of Directors declared a cash dividend of $0.14 per common share for the first quarter of fiscal 2010. The dividend is payable on June 3, 2009 to stockholders of record on May 13, 2009.

Issuer Purchases of Equity Securities

The Company did not repurchase any of its common stock during the fourth quarter of fiscal 2009. The value of shares or outstanding debentures that may yet be purchased under our current common stock and debentures repurchase program is $525.7 million. See Note 15. Stockholders Equity to our consolidated financial statements, included in Item 8. Financial Statements and Supplementary Data for information regarding our stock repurchase plans.

On February 25, 2008, we announced a repurchase program of up to $800.0 million of common stock. On November 6, 2008, our Board of Directors approved the amendment of the Company s $800.0 million stock repurchase program to provide that the funds may also be used to repurchase outstanding debentures. This repurchase program has no stated expiration date. Through March 28, 2009, the Company had used $274.3 million of the $800.0 million authorized for the repurchase of its outstanding common stock and debentures.

Company Stock Price Performance

The following graph shows a comparison of cumulative total return for the Company's common stock, the Standard & Poor's 500 Stock Index (S&P 500 Index), and the Standard & Poor's 500 Semiconductors Index (S&P 500 Semiconductors Index). The graph covers the period from April 2, 2004, the last trading day before Xilinx's 2005 fiscal year, to March 27, 2009, the last trading day of Xilinx's 2009 fiscal year. The graph and table assume that $100 was invested on April 2, 2004 in Xilinx, Inc. common stock, the S&P 500 Index and the S&P 500 Semiconductors Index and that all dividends were reinvested.

Company / Index	4/2/04	4/1/05	3/31/06	3/30/07	3/28/08	3/27/09
Xilinx, Inc.	**100.00**	72.47	64.79	66.44	60.79	52.73
S&P 500 Index	**100.00**	104.55	117.58	131.49	124.11	79.01
S&P 500 Semiconductors Index	**100.00**	80.37	88.16	81.40	76.20	56.39

Note: **Stock price performance and indexed returns for our Common Stock are historical and are not an indicator of future price performance or future investment returns.**

ITEM 6. SELECTED FINANCIAL DATA

Consolidated Statement of Income Data
Five years ended March 28, 2009
(In thousands, except per share amounts)

	2009(1)	2008(2)	2007(3)	2006(4)	2005(5)
Net revenues	$ 1,825,184	$ 1,841,372	$ 1,842,739	$ 1,726,250	$ 1,573,233
Operating income (6)	429,518	424,194	347,767	412,062	372,040
Income before income taxes (6)	498,184	474,094	431,146	456,602	400,544
Provision for income taxes	122,544	100,047	80,474	102,453	87,821
Net income	375,640	374,047	350,672	354,149	312,723
Net income per common share:					
Basic	$ 1.36	$ 1.27	$ 1.04	$ 1.01	$ 0.90
Diluted	$ 1.36	$ 1.25	$ 1.02	$ 1.00	$ 0.87
Shares used in per share calculations:					
Basic	276,113	295,050	337,920	349,026	347,810
Diluted	276,854	298,636	343,636	355,065	358,230
Cash dividends declared per common share	$ 0.56	$ 0.48	$ 0.36	$ 0.28	$ 0.20

(1) Income before income taxes includes restructuring charges of $22,023, a gain on early extinguishment of convertible debentures of $110,606, impairment loss on investments of $54,129 and a charge of $3,086 related to an impairment of a leased facility that the Company no longer intends to occupy.

(2) Income before income taxes includes a loss on the sale of the Company's remaining UMC investment of $4,732, an impairment loss on investments of $2,850 and a charge of $1,614 related to an impairment of a leased facility that the Company no longer intends to occupy.

(3) Income before income taxes includes a charge of $5,934 related to an impairment of a leased facility that the Company no longer intends to occupy, a loss related to a litigation settlement of $2,500, stock-based compensation related to prior years of $2,209, an impairment loss on investments of $1,950 and a gain of

$7,016 from the sale of a portion of the Company's UMC investment.

(4) Income before income taxes includes a loss related to litigation settlements and contingencies of $3,165, a write-off of acquired in-process R&D of $4,500 related to the acquisition of AccelChip and an impairment loss on investments of $1,418.

(5) Income before income taxes includes a write-off of acquired in-process R&D of $7,198 related to the acquisition of Hier Design Inc. and impairment loss on investments of $3,099.

(6) The Company adopted the provisions of Statement of Financial Accounting Standards (SFAS) No. 123(R), "Share-Based Payment" (SFAS 123(R)) in fiscal 2007. Results for prior fiscal years do not include the effects of stock-based compensation (see Notes 2 and 6 to our consolidated financial statements included in Item 8. "Financial Statements and Supplementary Data").

Consolidated Balance Sheet Data
Five years ended March 28, 2009
(In thousands)

	2009	2008	2007	2006	2005
Working capital	$ 1,519,402	$ 1,479,530	$ 1,396,733	$ 1,303,224	$ 1,154,163
Total assets	2,825,515	3,137,107	3,179,355	3,173,547	3,039,196
Convertible debentures	690,125	999,851	999,597		
Other long-term liabilities	81,776	40,281(1)	1,320	7,485	
Stockholders' equity	1,737,900	1,671,823	1,772,740	2,728,885	2,673,508

(1) Includes $39,122 of long-term income taxes payable reclassified from current to non-current liabilities in connection with the adoption of FIN 48. See "Note 16. Income Taxes" to our consolidated financial statements included in Item 8. "Financial Statements and Supplementary Data."

ITEM 7. MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS

This discussion and analysis of financial condition and results of operations should be read in conjunction with the Company's consolidated financial statements and accompanying notes included in Item 8. "Financial Statements and Supplementary Data."

Cautionary Statement

The statements in this Management's Discussion and Analysis that are forward looking, within the meaning of the Private Securities Litigation Reform Act of 1995, involve numerous risks and uncertainties and are based on current expectations. The reader should not place undue reliance on these forward-looking statements. Our actual results could differ materially from those anticipated in these forward-looking statements for many reasons, including those risks discussed under "Risk Factors" and elsewhere in this document. Often, forward-looking statements can be identified by the use of forward-looking words, such as "may," "will," "could," "should," "expect," "believe," "anticipate," "estimate," "continue," "plan," "intend," "project" and other similar terminology, or the negative of such terms. We disclaim any responsibility to update or revise any forward-looking statement provided in this Management's Discussion and Analysis for any reason.

Nature of Operations

We design, develop and market complete programmable logic solutions, including advanced ICs, software design tools, predefined system functions delivered as IP cores, design services, customer training, field engineering and technical support. Our PLDs include FPGAs and CPLDs. These devices are standard products that our customers program to perform desired logic functions. Our products are designed to provide high integration and quick time-to-market for electronic equipment manufacturers in end markets such as wired and wireless communications, industrial, scientific and medical, aerospace and defense, audio, video and broadcast, consumer, automotive and data processing. We sell our products globally through independent domestic and foreign distributors and through direct sales to OEMs by a network of independent sales representative firms and by a

direct sales management organization.

Critical Accounting Policies and Estimates

The methods, estimates and judgments we use in applying our most critical accounting policies have a significant impact on the results we report in our consolidated financial statements. The SEC has defined critical accounting policies as those that are most important to the portrayal of our financial condition and results of operations and require us to make our most difficult and subjective judgments, often as a result of the need to make estimates of matters that are inherently uncertain. Based on this definition, our critical accounting policies include: valuation of marketable and non-marketable securities, which impacts losses on debt and equity securities when we record impairments; revenue recognition, which impacts the recording of revenues; and valuation of inventories, which impacts cost of revenues and gross margin. Our critical accounting policies also include: the assessment of impairment of long-lived assets including acquisition-related intangibles, which impacts their valuation; the assessment of the recoverability of goodwill, which impacts goodwill impairment; accounting for income taxes, which impacts the provision or benefit recognized for income taxes, as well as the valuation of deferred tax assets recorded on our consolidated balance sheet; and valuation and recognition of stock-based compensation, which impacts gross margin, R&D expenses, and selling, general and administrative (SG&A) expenses. Below, we discuss these policies further, as well as the estimates and judgments involved. We also have other key accounting policies that are not as subjective, and therefore, their application would not require us to make estimates or judgments that are as difficult, but which nevertheless could significantly affect our financial reporting.

Valuation of Marketable and Non-marketable Securities

The Company's short-term and long-term investments include marketable debt securities and non-marketable equity securities. As of March 28, 2009, the Company had marketable debt securities with a fair value of $1.24 billion and non-marketable equity securities in private companies of $20.5 million (adjusted cost).

Beginning in the first quarter of fiscal 2009, the assessment of fair value is based on the provisions of SFAS No. 157, "Fair Value Measurements" (SFAS 157). The Company determines the fair values for marketable debt and equity securities using industry standard pricing services, data providers and other third-party sources and by performing valuation analyses. See "Note 3. Fair Value Measurements" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data," for details of the valuation methodologies. In determining if and when a decline in value below adjusted cost of marketable debt and equity securities is other than temporary, the Company evaluates on an ongoing basis the market conditions, trends of earnings, financial condition, credit ratings, any underlying collateral and other key measures for our investments. We assess other-than-temporary impairment of debt and equity securities in accordance with FASB Staff Position (FSP) No. FAS 115-1, "The Meaning of Other-Than-Temporary Impairment and Its Application to Certain Investments." We recorded other-than-temporary impairments for marketable debt securities and a marketable equity security in fiscal 2009. We did not record any other-than-temporary impairment for marketable debt or equity securities in fiscal 2008 or 2007.

The Company's investments in non-marketable securities of private companies are accounted for by using the cost method. These investments are measured at fair value on a non-recurring basis when they are deemed to be other-than-temporarily impaired. In determining whether a decline in value of non-marketable equity investments in private companies has occurred and is other than temporary, an assessment is made by considering available evidence, including the general market conditions in the investee's industry, the investee's product development status and subsequent rounds of financing and the related valuation and/or our participation in such financings. We also assess the investee's ability to meet business milestones and the financial condition and near-term prospects of the individual investee, including the rate at which the investee is using its cash and the investee's need for possible additional funding at a lower valuation. Beginning in the first quarter of fiscal 2009, the assessment of fair value is based on the provisions of SFAS 157. The valuation methodology for determining the decline in value of non-marketable equity securities is based on the factors noted above which require management judgment and are Level 3 inputs. See "Note 3. Fair Value Measurements" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data," for additional information relating to the adoption of SFAS 157. When a decline in value is deemed to be other than temporary, the Company recognizes an impairment loss in the current period's operating results to the extent of the decline. We recorded other-than-temporary impairments for non-marketable equity securities in fiscal 2009, 2008 and

2007.

Revenue Recognition

Sales to distributors are made under agreements providing distributor price adjustments and rights of return under certain circumstances. Revenue and costs relating to distributor sales are deferred until products are sold by the distributors to the distributors end customers. For fiscal 2009, approximately 77% of our net revenues were from products sold to distributors for subsequent resale to OEMs or their subcontract manufacturers. Revenue recognition depends on notification from the distributor that product has been sold to the distributor s end customer. Also reported by the distributor are product resale price, quantity and end customer shipment information, as well as inventory on hand. Reported distributor inventory on hand is reconciled to deferred revenue balances monthly. We maintain system controls to validate distributor data and to verify that the reported information is accurate. Deferred income on shipments to distributors reflects the effects of distributor price adjustments and the amount of gross margin expected to be realized when distributors sell through product purchased from the Company. Accounts receivable from distributors are recognized and inventory is relieved when title to inventories transfers, typically upon shipment from Xilinx at which point we have a legally enforceable right to collection under normal payment terms.

As of March 28, 2009, we had $90.4 million of deferred revenue and $28.0 million of deferred cost of goods sold recognized as a net $62.4 million of deferred income on shipments to distributors. As of March 29, 2008, we had $158.0 million of deferred revenue and $46.3 million of deferred cost of goods sold recognized as a net $111.7 million of deferred income on shipments to distributors. The deferred income on shipments to distributors that will ultimately be recognized in our consolidated statement of income will be different than the amount shown on the consolidated balance sheet due to actual price adjustments issued to the distributors when the product is sold to their end customers.

Revenue from sales to our direct customers is recognized upon shipment provided that persuasive evidence of a sales arrangement exists, the price is fixed, title has transferred, collection of resulting receivables is reasonably assured, and there are no customer acceptance requirements and no remaining significant obligations. For each of the periods presented, there were no significant formal acceptance provisions with our direct customers.

Revenue from software licenses is deferred and recognized as revenue over the term of the licenses of one year. Revenue from support services is recognized when the service is performed. Revenue from Support Products, which includes software and services sales, was less than 7% of net revenues for all of the periods presented.

Allowances for end customer sales returns are recorded based on historical experience and for known pending customer returns or allowances.

Valuation of Inventories

Inventories are stated at the lower of actual cost (determined using the first-in, first-out method) or market (estimated net realizable value). The valuation of inventory requires us to estimate excess or obsolete inventory as well as inventory that is not of saleable quality. We review and set standard costs quarterly to approximate current actual manufacturing costs. Our manufacturing overhead standards for product costs are calculated assuming full absorption of actual spending over actual volumes, adjusted for excess capacity. Given the cyclicality of the market, the obsolescence of technology and product lifecycles, we write down inventory based on forecasted demand and technological obsolescence. These factors are impacted by market and economic conditions, technology changes, new product introductions and changes in strategic direction and require estimates that may include uncertain elements. The estimates of future demand that we use in the valuation of inventory are the basis for our published revenue forecasts, which are also consistent with our short-term manufacturing plans. If our demand forecast for specific products is greater than actual demand and we fail to reduce manufacturing output accordingly, we could be required to write down additional inventory, which would have a negative impact on our gross margin.

Impairment of Long-Lived Assets Including Acquisition-Related Intangibles

Long-lived assets and certain identifiable intangible assets to be held and used are reviewed for impairment if indicators of potential impairment exist. Impairment indicators are reviewed on a quarterly basis. When indicators of impairment exist and assets are held for use, we estimate future undiscounted cash flows attributable to the assets. In the event such cash flows are not expected to be sufficient to recover the recorded value of the assets, the assets are written down to their estimated fair values based on the expected discounted future cash flows attributable to the assets or based on appraisals. Factors affecting impairment of assets held for use include the ability of the specific assets to generate positive cash flows.

When assets are removed from operations and held for sale, we estimate impairment losses as the excess of the carrying value of the assets over their fair value. Factors affecting impairment of assets held for sale include market conditions. Changes in any of these factors could necessitate impairment recognition in future periods for assets held for use or assets held for sale.

Long-lived assets such as goodwill, other intangible assets and property, plant, and equipment, are considered nonfinancial assets, and are only measured at fair value when indicators of impairment exist. The accounting and disclosure provisions of SFAS 157 will not be effective for these assets until the first quarter of fiscal 2010. See "Note 3. Fair Value Measurements" to our consolidated financial statements, included in Item 8. "Financial Statements and Supplementary Data," for additional information.

Goodwill

As required by SFAS No. 142, "Goodwill and Other Intangible Assets" (SFAS 142), goodwill is not amortized but is subject to impairment tests on an annual basis, or more frequently if indicators of potential impairment exist, and goodwill is written down when it is determined to be impaired. We perform an annual impairment review in the fourth quarter of each fiscal year and compare the fair value of the reporting unit in which the goodwill resides to its carrying value. If the carrying value exceeds the fair value, the goodwill of the reporting unit is potentially impaired. For purposes of impairment testing under SFAS 142, Xilinx operates as a single reporting unit. We use the quoted market price method to determine the fair value of the reporting unit. Based on the impairment review performed during the fourth quarter of fiscal 2009, there was no impairment of goodwill in fiscal 2009. Unless there are indicators of impairment, our next impairment review for goodwill will be performed and completed in the fourth quarter of fiscal 2010. To date, no impairment indicators have been identified.

Accounting for Income Taxes

Xilinx is a multinational corporation operating in multiple tax jurisdictions. We must determine the allocation of income to each of these jurisdictions based on estimates and assumptions and apply the appropriate tax rates for these jurisdictions. We undergo routine audits by taxing authorities regarding the timing and amount of deductions and the allocation of income among various tax jurisdictions. Tax audits often require an extended period of time to resolve and may result in income tax adjustments if changes to the allocation are required between jurisdictions with different tax rates.

In determining income for financial statement purposes, we must make certain estimates and judgments. These estimates and judgments occur in the calculation of certain tax liabilities and in the determination of the recoverability of certain deferred tax assets, which arise from temporary differences between the tax and financial statement recognition of revenue and expense. Additionally, we must estimate the amount and likelihood of potential losses arising from audits or deficiency notices issued by taxing authorities. The taxing authorities' positions and our assessment can change over time resulting in a material effect on the provision for income taxes in periods when these changes occur.

We must also assess the likelihood that we will be able to recover our deferred tax assets. If recovery is not likely, we must increase our provision for taxes by recording a reserve in the form of a valuation allowance for the deferred tax assets that we estimate will not ultimately be recoverable.

The Company has elected to adopt the alternative transition method provided in FSP No. FAS 123(R)-3, "Transition Election Related to Accounting for the Tax Effects of Share-Based Payment Awards" for calculating the tax effects of stock-based compensation pursuant to SFAS 123(R). The alternative transition method includes simplified methods to establish the beginning balance of the APIC pool related to the tax effects of employee stock-based compensation, and to determine the subsequent impact on the APIC pool and consolidated statements of cash flows of the tax effects of employee stock-based compensation awards that are outstanding

upon adoption of SFAS 123(R).

In June 2006, the FASB issued FIN 48. FIN 48 contains a two-step approach to recognizing and measuring uncertain tax positions accounted for in accordance with SFAS No. 109, Accounting for Income Taxes (SFAS 109). The first step is to evaluate the tax position for recognition by determining if the weight of available evidence indicates that it is more likely than not that the position will be sustained on audit, including resolution of related appeals or litigation processes, if any. The second step is to measure the tax

benefit as the largest amount that is more than 50% likely of being ultimately realized. See Note 16. Income Taxes to our consolidated financial statements included in Item 8. Financial Statements and Supplementary Data.

Stock-Based Compensation

In the first quarter of fiscal 2007, we adopted SFAS 123(R), which requires the measurement at fair value and recognition of compensation expense for all stock-based payment awards. Determining the appropriate fair-value model and calculating the fair value of stock-based awards at the date of grant requires judgment. We use the Black-Scholes option-pricing model to estimate the fair value of employee stock options and rights to purchase shares under the Company s Employee Stock Purchase Plan, consistent with the provisions of SFAS 123(R). Option pricing models, including the Black-Scholes model, also require the use of input assumptions, including expected stock price volatility, expected life, expected dividend rate, expected forfeiture rate and expected risk-free rate of return. We use implied volatility based on traded options in the open market as we believe implied volatility is more reflective of market conditions and a better indicator of expected volatility than historical volatility. In determining the appropriateness of implied volatility, we considered: the volume of market activity of traded options, and determined there was sufficient market activity; the ability to reasonably match the input variables of traded options to those of options granted by the Company, such as date of grant and the exercise price, and determined the input assumptions were comparable; and the length of term of traded options used to derive implied volatility, which is generally one to two years and which was extrapolated to match the expected term of the employee options granted by the Company, and determined the length of the option term was reasonable. The expected life of options granted is based on the historical exercise activity as well as the expected disposition of all options outstanding. We will continue to review our input assumptions and make changes as deemed appropriate depending on new information that becomes available. Higher volatility and expected lives result in a proportional increase to stock-based compensation determined at the date of grant. The expected dividend rate and expected risk-free rate of return do not have as significant an effect on the calculation of fair value.

In addition, SFAS 123(R) requires us to develop an estimate of the number of stock-based awards which will be forfeited due to employee turnover. Quarterly changes in the estimated forfeiture rate have an effect on reported stock-based compensation, as the effect of adjusting the rate for all expense amortization after April 1, 2006 is recognized in the period the forfeiture estimate is changed. If the actual forfeiture rate is higher than the estimated forfeiture rate, then an adjustment is made to increase the estimated forfeiture rate, which will result in a decrease to the expense recognized in the financial statements. If the actual forfeiture rate is lower than the estimated forfeiture rate, then an adjustment is made to decrease the estimated forfeiture rate, which will result in an increase to the expense recognized in the financial statements. The effect of forfeiture adjustments in fiscal 2009, 2008 and 2007 was insignificant. The expense we recognize in future periods could also differ significantly from the current period and/or our forecasts due to adjustments in the assumed forfeiture rates.

Results of Operations

The following table sets forth statement of income data as a percentage of net revenues for the fiscal years indicated:

	2009	2008	2007
Net Revenues	**100.0%**	**100.0%**	**100.0%**
Cost of revenues	36.7	37.3	39.0
Gross Margin	**63.3**	**62.7**	**61.0**
Operating Expenses:			

Research and development	19.5	19.4	21.1
Selling, general and administrative	18.8	19.9	20.4
Amortization of acquisition-related intangibles	0.3	0.4	0.4
Restructuring charges	1.2	0.0	0.0
Litigation settlement	0.0	0.0	0.1
Stock-based compensation related to prior years	0.0	0.0	0.1
Total operating expenses	39.8	39.7	42.1
Operating Income	**23.5**	**23.0**	**18.9**
Gain on early extinguishment of convertible debentures	6.1	0.0	0.0
Impairment loss on investments	(3.0)	(0.2)	(0.1)
Interest and other income, net	0.7	2.9	4.6
Income Before Income Taxes	**27.3**	**25.7**	**23.4**
Provision for income taxes	6.7	5.4	4.4
Net Income	**20.6%**	**20.3%**	**19.0%**

Net Revenues

(In millions)	2009	Change	2008	Change	2007
Net revenues	$1,825.2	(1)%	$1,841.4	0%	$1,842.7

The 1% decline in net revenues in fiscal 2009 compared to fiscal 2008 was largely due to the recessionary environment we experienced during the fiscal year which impacted our sales across a broad base of end markets. New Product revenue increased considerably in fiscal 2009 but not enough to fully offset the declines in Base and Mainstream Products. Total unit sales declined in fiscal 2009 but average selling price per unit increased compared to the comparable prior year period. The relatively flat net revenues in fiscal 2008 compared to fiscal 2007 was driven by strong customer demand for our New Products which was offset by decreased demand for our Mainstream and Base Products, particularly in the Communications and Data Processing end markets. Increased total unit sales during fiscal 2008 compared to the comparable prior year period were offset by declines in average unit selling prices, which also contributed to the flat net revenues in fiscal 2008. See "Net Revenues by Product" and "Net Revenues by End Markets" below for more information on our product and end-market categories.

No end customer accounted for more than 10% of net revenues for any of the periods presented.

Net Revenues by Product

We classify our product offerings into four categories: New, Mainstream, Base and Support Products. These product categories, excluding Support Products, are modified on a periodic basis to better reflect advances in technology. The most recent adjustment was made on July 2, 2006, which was the beginning of our second quarter of fiscal 2007. New Products, as currently defined, include our most recent product offerings and include the Virtex-5, Virtex-4, Spartan-3 and CoolRunner-II product families. Mainstream Products include the Virtex-II, Spartan-II, CoolRunner and Virtex-E product families. Mainstream products are generally several years old and designed into customer programs that are currently shipping in full production. Base Products consist of our older product families including the Virtex, Spartan, XC4000 and XC9500 products. Support Products make up the remainder of our product offerings and include configuration products, software, IP cores, customer training, design services and support. In fiscal 2010, we expect to reclassify our net revenues by product categories to better reflect the age of the products and advances in technologies.

Net revenues by product categories for the fiscal years indicated were as follows:

(In millions)	2009	% of Total	% Change	2008	% of Total	% Change	2007	% of Total
New Products	$ 847.9	47	40	$604.2	33	45	$ 416.8	23
Mainstream Products	673.0	37	(21)	849.8	46	(15)	1,004.2	54
Base Products	206.3	11	(26)	277.7	15	(12)	317.2	17
Support Products	98.0	5	(11)	109.7	6	5	104.5	6
Total net revenues	$1,825.2	100						